Clean Version of the Entire Set of Pending Claim

1-12. (Cancelled)

13. (Amended) A method for assembling an electronic package, comprising:

forming a housing which has a bond pad located on a first surface of a bond shelf, the bond shelf having a second surface along the thickness of the bond shelf;

forming a conductive strip along the second surface of the bond shelf; and

removing a portion of the conductive strip.

14. (Amended) The method as recited in claim 13, wherein the conductive strip is formed by plating a conductive material onto the second surface.

15. The method as recited in claim 13, wherein the portion of the conductive strip is removed by drilling a portion of the bond shelf.

16. The method as recited in claim 13, further comprising:

mounting an integrated circuit to the housing and connecting the integrated circuit to the bond pad.

17. (Amended) The method as recited in claim 13, wherein the portion of the conductive strip is removed by etching away a portion of a conductive material on the second surface of the bond shelf.

18. (Amended) The method as recited in claim 13, wherein the conductive strip is formed along the second surface of the bond shelf by masking all surfaces of the bond shelf except for the second surface of the bond shelf, and plating a conductive material onto the second surface of the bond shelf.

19. The method as recited in claim 18, wherein the conductive material is copper, and the conductive strip is further formed by plating gold onto the copper.

20. The method as recited in claim 19, wherein

the portion of the conductive strip is removed by drilling a portion of the bond shelf.

21. (Amended) A method of forming an integrated circuit package, comprising:

providing a package housing having a first plurality of bonding pads located on a first surface of a first bond shelf, the first bond shelf having a second surface along the thickness of the bond shelf;

forming a first conductive strip along the second surface of the first bond shelf, the first conductive strip wrapping around a first edge of the first bond shelf to at least one of the first plurality of bonding pads on the first surface of the first bond shelf, the at least one of the first plurality of bonding pads coupled to a first conductor under the first bond shelf; and,

removing a portion of the first conductive strip.

22. (Amended) The method as recited in claim 21, wherein the first conductive strip is formed by plating a conductive material onto the second surface.

23. The method as recited in claim 21, wherein the first conductor under the first bond shelf is a power bus.

24. The method as recited in claim 21, wherein the first conductor under the first bond shelf is a routing trace.

25. The method as recited in claim 21, wherein the portion of the first conductive strip is removed by drilling a portion of the first bond shelf.

26. The method as recited in claim 25, wherein the portion drilled in the first bond shelf is a notch.

27. (Amended) The method as recited in claim 21, wherein the portion of the first conductive strip is removed by etching away a portion of the first conductive strip on the second surface of the first bond shelf.

28. The method as recited in claim 21, wherein the package housing is provided by

forming a first conductive layer on a first dielectric substrate,

placing a second dielectric substrate on the first conductive layer of the first dielectric substrate, the second dielectric substrate having a second conductive layer, and

etching the second conductive layer to form the first plurality of bonding pads.

29. The method as recited in claim 28, wherein

the first conductive layer forms the first conductor under the first bond shelf.

30. (Amended) The method as recited in claim 28, wherein

the etching of the second conductive layer to further form a second conductor, and

the package housing has a second plurality of bonding pads located on a first surface of the second bond shelf, the second bond shelf having a second surface along the thickness of the second bond shelf, the package housing is further provided by

placing a third dielectric substrate on the second conductive layer of the second dielectric substrate, the third dielectric substrate having a third

conductive layer, and

etching the third conductive layer to form a second plurality of bonding pads, and

the method further includes

forming a second conductive strip along the second surface of the second bond shelf, the second conductive strip wrapping around a first edge of the second bond shelf to at least one of the second plurality of bonding pads on the first surface of the second bond shelf, the at least one of the first plurality of bonding pads on the first surface of the second bond shelf coupled to the second conductor under the second bond shelf.

31. The method as recited in claim 30, wherein

the second conductive layer forms the second conductor under the second bond shelf.

32. (Amended) The method as recited in claim 30, wherein

the second conductive strip is formed by plating a conductive material onto the second surface of the second bond shelf.

33. The method as recited in claim 30, wherein the second conductor under the second bond shelf is a power bus.

34. The method as recited in claim 30, wherein the second conductor under the second bond shelf is a routing trace.

Add E5